REMARKS

This responds to the Office Action mailed on December 13, 2007.

Claim 19 is amended, no claims are canceled, and no claims are added; as a result, claims 19-24, 51-61 and 88-89 are now pending in this application.

§103 Rejection of the Claims

Claims 19, 21-24, 51-54, 56-58, 60-61 and 88-89 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,898,858 to Gillespie (hereinafter, "the Gillespie reference") in view of U.S. Patent No. 6,121,689 to Capote *et al.* (hereinafter, "the Capote reference") and U.S. Patent No. 5,528,080 to Goldstein (hereinafter, "the Goldstein reference"). Claims 20, 55 and 59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Gillespie reference in view of the Capote reference and the Goldstein reference as applied to claim 19 above, and further in view of U.S. Patent No. 6,337,257 to Toyosawa *et al.* (hereinafter, "the Toyosawa reference"). Applicants disagree with the foregoing stated grounds of rejection and desire to further clarify various distinctions of the present invention over the cited art. Reconsideration of the present application is therefore requested in light of the present amendment and following remarks.

In the following discussion, the disclosed embodiments of the invention may be discussed in comparison to the prior art. It is understood, however, that any discussion of the disclosed embodiments, as well as any discussion of the differences between the disclosed embodiments of the present invention and the prior art do not define the scope or interpretation of any of the claims. Instead, such discussed differences, if presented, are offered merely to help the Examiner appreciate important claim distinctions as they are discussed.

The Examiner has cited the Gillespie reference for allegedly disclosing an electronic system having a processor, memory controller and a memory device coupled to the memory controller that includes a ball grid array (BGA) chip package. The Examiner acknowledges, however, that the Gillespie reference fails to explicitly disclose that the chip package associated with the memory device includes a adhesive layer, an array of columnar openings that are aligned with connection pads on the chip package, a chamfer in the adhesive layer at each of the openings, and a conductive material positioned in the openings.

Accordingly, the Examiner cites the Capote reference for this necessary teaching. Specifically, the Examiner cites a flip-chip structure shown in Figures 3, 6 and 7. Applicant notes that the disclosed vias extending through the encapsulant do not include a chamfer, or any other type of configured edge formed in the vias.

The Examiner has also cited the Goldstein reference for disclosing an array of columnar openings in a semiconductor material that allegedly include a chamfer. With reference now specifically to Figure 20 (which is the "cover" figure referred to by the Examiner on page 3 of the Office Action), the disclosed structure includes a semiconductor material 91 that has recesses 88 having a dimension 89 that give the appearance of a chamfer formed in the semiconductor material 91. Applicant notes that the conductive interconnections 94 that extend into the alleged chamfer (*e.g.*, the recess 88) do not extend through the recess 88. Hence, the conductive interconnections 94 could not extend to conductive pads positioned on a chip. Accordingly, the proposed combination would yield an apparatus that is unsuitable for its intended purpose, since the conductive interconnections 94 could not conductively communicate with an adjacent chip.

If the Examiner asserts that the Capote reference provides the necessary teaching that conductive members extend through the recesses 88 disclosed in the Goldstein reference, Applicant responds that the two teachings are simply inconsistent. For example, the Goldstein reference discloses that the recesses 88 are formed in the semiconductor material 91 along a <111> plane using an orientation dependent etching method. Applicant cannot see how the disclosed formation method is relevant to a chamfer formed in a polymeric material.

Turning now to the claims, differences between the claim language, and the applied references will be specifically pointed out. Claim 19, as amended, recites in pertinent part: "An electronic system comprising... an adhesive layer...having a chamfer...opposite the first surface of the adhesive layer at a second surface of the adhesive layer at each of the column-shaped openings; and...at least one of the array of column-shaped openings includes a conductive material forming a conductive column within the at least one column-shaped opening, the conductive material in direct contact with the adhesive layer *and extending through the chamfer to the first surface of the adhesive layer* within the column shaped opening." (Emphasis added). The asserted combination of references simply does not disclose or fairly suggest this. In particular, Applicant notes that the teachings of the Capote and Goldstein references cannot be

properly combined, since the structure 80 (Figure 20 of the Goldstein reference) includes conductive members adjacent the recesses 88 that cannot establish electrical communication with a semiconductor chip. The combination thus yields a structure inoperable to perform its intended purpose. Still further, Applicant fails to understand how the semiconductor etching process disclosed in the Goldstein reference is applicable to a polymeric material, much less effective applied to such materials.

Claim 19 is therefore allowable over the cited combination of references. Claims 21-24, 51-54, 56-58, 60-61 and 88-89, which depend from claim 19, are also allowable, based upon the allowable form of the base claim, and further in view of the additional limitations recited in the dependent claims.

The Examiner has also cited the Toyosawa reference as pertinent to the patentability of claims 20, 55 and 59. Specifically, the Examiner has applied the Toyosawa reference for disclosing a protective tape applied to second side of a semiconductor chip. Applicant submits that the teaching in the Toyosawa reference fails to provide the teaching missing from Gillespie, Capote and Goldstein references. Applicant accordingly requests that the rejection of claims 20, 55 and 59 be withdrawn.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 4/14/08

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 14th day of April 2008.

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